REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 3-6 and 8-12 are presently active in this case. Claims 3-6, 9, and 10 are amended and Claims 1, 2, 7, and 11 are canceled without prejudice or disclaimer by way of the present amendment. Support for the amendments can be found in the original claims.

In the outstanding Office Action, Claims 1-3, 5-7, and 9-11 were rejected under 35 U.S.C. § 102(b) as anticipated by Tomassi, et al. (U.S. Patent No. 5,606,707, herein "Tomassi"). Claims 4, 8, and 12 were rejected under 35 U.S.C. § 103(a) as unpatentable over Tomassi in view of Johnson, et al. (U.S. Patent No. 5,253,308, herein "Johnson").

Applicants and Applicants' representative wish to thank Examiner Lamb for the interview granted on November 24, 2004. During that interview, the outstanding rejections were discussed in detail. Further, during the interview arguments as hereinafter discussed were presented. During the interview Examiner Lamb indicated that she would review the cited references in view of such arguments and, if necessary, would update her search when such arguments are formally presented in a filed response.

In regard to the rejection of Claims 1, 2, 7, and 11 under 35 U.S.C. § 102(b) as anticipated by Tomassi, Applicants cancel Claims 1, 2, 7, and 11 rendering the rejection of these claims moot.

In regard to the rejection of Claims 3, 5, 6, 9, and 10 under 35 U.S.C. § 102(b) as anticipated by Tomassi, Applicants respectfully traverse the rejection for the following reasons.

Claim 3 recites an image processing apparatus which refers to peripheral pixels of a target pixel to perform processing of said target pixel, wherein an effective number of pixels

obtained by subtracting the number of peripheral pixels from the number of batch processed pixels is a multiple of the number of rows or columns of a dither matrix and an integer.

Tomassi does not disclose or suggest the above-mentioned effective number feature of Claim 1. The outstanding Office Action cites column 7, lines 43-53 of Tomassi to meet the claim feature of the effective number; however, as discussed during the interview the above-mentioned relation between the effective number and the number of rows or columns of a dither matrix of Claim 1 is not disclosed in Tomassi.

Accordingly, Applicants respectfully submit that the rejection of Claim 3 under 35 U.S.C. § 102(b) should be withdrawn.

Claim 5, as amended, recites an image processing apparatus comprising, *inter alia*, an input I/F memory configured to read pixels having a predetermined length at a first speed, subject these pixels to buffering, and write the pixels in a SIMD type processor at a second speed, the second speed being faster than the first speed; and an output I/F memory configured to read batch processed pixels from an SIMD type processor at a third speed, subject the batch processed pixels to buffering, and write the batch processed pixels in a predetermined output destination at a fourth speed, the fourth speed being slower than the third speed.

Tomassi does not disclose or suggest the above-mentioned input I/F memory feature of Claim 5, as amended. The outstanding Office Action cites column 8, lines 9-20 to meet the claim feature of input the I/F memory; however, the above-mentioned input I/F memory feature of Claim 5, as amended, is not disclosed in Tomassi. In Tomassi, "IBIB FIFO 211 and OBIB FIFO 213 each buffer image data"[1]; however, Tomassi is silent as to writing pixels in a SIMD type processor at a speed faster than that of reading the pixels, as recited in Claim 5, as amended.

[1] Column 8, lines 18-29 of Tomassi.

Tomassi does not disclose or suggest the above-mentioned output I/F memory feature of Claim 5, as amended. The outstanding Office Action recites column 8, lines 21-27 to meet the claim feature of output I/F memory; however, the above-mentioned output I/F memory feature of Claim 5, as amended, is not disclosed in Tomassi. In Tomassi, "the data on the NCM bus 209 is clocked into an OBOB FIFO 217"[2] and the output of the OBOB FIFO 217 may be clocked into the output buffer 203"[3]; however, Tomassi is silent as to writing batch processed pixels in a predetermined output destination at a speed slower than that of reading of the batch processed pixels, as recited in Claim 5, as amended.

Accordingly, Applicants respectfully submit that the rejection of Claim 5 under 35 U.S.C. § 102(b) should be withdrawn.

Independent Claim 9 includes recitations similar to those in Claim 5 discussed above. Claims 6 and 10 depend on Claim 5 or 9. Accordingly, Applicants respectfully submit that Claims 6, 9, and 10 are allowable at least for the reasons given above with respect to Claim 5 in addition to the novel and non-obvious features recited therein.

In regard to the rejection of Claims 4, 8, and 12 under 35 U.S.C. § 103(a) as unpatentable over Tomassi in view of Johnson, Applicants respectfully traverse the rejection for the following reasons.

Claim 4 recites an image processing apparatus which refers to peripheral pixels of a target pixel to perform processing of the target pixel, wherein an SIMD type processor is physically detachable from an input I/F memory or an output I/F memory.

The outstanding Office Action states that "Tomassi does not specifically teach wherein said SIMD type processor is physically detachable from said input I/F memory of said output I/F memory."[4] The outstanding Office Action cites column 12, lines 6-21 of Johnson to cure

[2] Column 8, lines 23-25 of Tomassi.
[3] Column 8, lines 26-27 of Tomassi.
[4] Page 5, Office Action of October 1, 2004

these deficiencies of Tomassi; however, Johnson does not teach or suggest an image processing apparatus, wherein an SIMD type processor is physically detachable from an input I/F memory or an output I/F memory, as recited in Claim 4, as amended. In Johnson,

> when a fault is detected in a certain processing element 202 or group thereof within the processing array 110, the bypass signal 626 may be activated for the column of chips 600 that contains the defective processing element(s) 202, thereby effectively removing the defective processing element(s) 202 from the active processing array 110. A redundant column of processing elements 202 can then be activated to replace the column containing the defective processing element(s) 202.[5]

In other words, in Johnson, when a fault is detected in a processing element, the column of processing elements that contains the defective processing element is deactivated. However, Johnson is silence as to physically detaching the defective processing element from an input I/F memory or an output I/F memory. Nowhere in Johnson teach or suggest an image processing apparatus, wherein an SIMD type processor is physically detachable from an input I/F memory or an output I/F memory, as recited in Claim 4.

Accordingly, Applicants respectfully submit that the rejection of Claim 4 under 35 U.S.C. § 103(a) should be withdrawn.

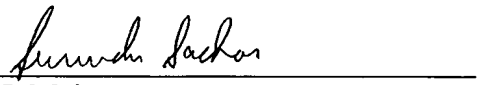
Claims 8 and 12 include recitations similar to those in Claim 4 discussed above. Furthermore, Claims 8 and 12 depend from Claim 5 or 9. As discussed above, Tomassi does not teach or suggest all features of Claims 5 and 9. Johnson does not cure these deficiencies. Accordingly, Applicants respectfully submit that rejection of Claims 8 and 12 under 35 U.S.C. § 103(a) should be withdrawn as well.

[5] Column 12, lines 12-21 of Johnson.

In view of the foregoing remarks, Applicants respectfully submit that each and every one of Claims 3-6 and 8-12 defines patentable subject matter, and that the application is in condition for allowance. Applicants respectfully request reconsideration and reexamination of this application and timely allowance of the pending claims.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Gregory J. Maier
Attorney of Record
Registration No. 25,599

Surinder Sachar
Registration No. 34,423

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/03)

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